decreasing the amount of signal transmission when an FET is in an OFF state as small as possible and of improving a variable ratio of the amount of signal transmission.

B2

Page 6, lines 7-12, please amend this paragraph as follows:

Thus, in the first preferred embodiment, the inductor element 1 is provided between the source terminal and ground terminal of the FET 10, and the inductor element 1 resonates in series for the gate-to-source impedance of the FET 10, so that it is possible to sufficiently decrease the amount of signal transmission when the FET 10 is in the OFF state.

B3

IN THE CLAIMS

Please amend Claims 1 and 11 as shown in clean form below. A marked-up copy of amended Claims 1 and 11 is attached.

1. (Amended) A semiconductor integrated circuit comprising:

an FET having a gate terminal configured to input a controlled signal and a drain terminal configured to output a signal corresponding to said controlled signal; and

an inductor element provided between a source terminal and a ground terminal of said FET,

wherein when a drain voltage of said FET is lower than a source voltage thereof, a series resonance circuit it formed of a reactance component of a gate-to-source impedance and said inductor element, and an inductance value of said inductor element is set in accordance with a frequency of said controlled signal.

B4

Sub C1

11. (Amended) A semiconductor integrated circuit comprising:

B5

Sub C2